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PATENT APPLICATION
Docket No. 11675.106

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT APPLICATION
Honorable Commissioner of Patents
and Trademarks
Washington, DC 20231

Sir:

Transmitted herewith for filing is the patent application of John H. Givens for UTILIZATION OF ENERGY ABSORBING LAYER TO IMPROVE METAL FLOW AND FILL IN A NOVEL INTERCONNECT STRUCTURE, comprising thirty-two (32) pages of specification and claims, and a single signature Declaration, Power of Attorney and Petition.

- Enclosed also are:

X One (1) drawing sheet.

X An assignment of the invention to Micron Technology, Inc., including a Form PTO-1595 recordation cover sheet.

___ A certified copy of an _____ application.

___ An Associate Power of Attorney

___ A Verified Statement to Establish Small Entity Status Under 37 C.F.R. § 1.9 and 37 C.F.R. § 1.27

X A Certificate of Mailing by "Express Mail" certifying a filing date of February 14, 1997, by use of Express Mail Label No. EM246228404US.

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The filing fee has been calculated as shown below.

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| BASIC FEE | | | | $ 385 | | | $ 770 |
| TOT. CLAIMS | 35-20= | 15 | X 11= | $ | OR | X 22= | $ 330 |
| IND. CLAIMS | 8-3= | 5 | X 40= | $ | OR | X 80= | $ 400 |
| MULTIPLE DEPENDENT CLAIM PRESENTED | | | +130= | $ | OR | +260= | $ |
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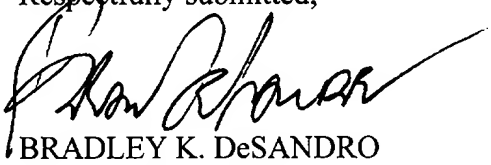
X The issue fee set forth in 37 C.F.R. § 1.18 at or before mailing of the Notice of Allowance, pursuant to 37 C.F.R. § 1.311(b).

X Any filing fees under 37 C.F.R. § 1.16 for presentation of extra claims.

Please address all future correspondence in connection with the above-identified patent application to the attention of the undersigned.

Dated this 14th day of February, 1997.

Respectfully submitted,



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PATENT APPLICATION
Docket No. 11675.106

**UNITED STATES PATENT APPLICATION**

of

**JOHN H. GIVENS**

for

# UTILIZATION OF ENERGY ABSORBING LAYER TO IMPROVE METAL FLOW AND FILL IN A NOVEL INTERCONNECT STRUCTURE

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## BACKGROUND OF THE INVENTION

### 1. The Field of the Invention

The present invention relates to a metallized integrated circuit structure, and particularly to a metallized interconnect structure situated on a semiconductor substrate assembly and methods for making.

### 2. The Relevant Technology

Current technology for metallization of an integrated circuit involves the forming of a conductive layer over the integrated circuit. A typical metallization process is one that is performed at the "back end of the line" which is after the formation of integrated circuits that are to be wired by the metallization process. A single conductive layer is often formed so that it is situated above the integrated circuit to be wired. After the conductive layer is formed, it is then patterned and etched into a shape of the desired wiring necessary to metallize the integrated circuit. Since the conductive layer is situated above the integrated circuit, the resultant metallization will also be above the integrated circuit in a "wiring up" scheme.

Another type of metallization involves the formation of a conductive layer at least in part below the integrated circuit in a recess composed of an electrically insulative or dielectric material. Such a wiring scheme may be described as a "wiring down" scheme. The recess can be either a trench, a hole, or a via. Depending upon the aspect ratio of the recess, poor step coverage of the conductive layer within the recess may result. Voids in the conductive layer within the recess may also result when the conductive layer does not completely fill up the recess. Voids and poor step coverage can cause the integrated circuit to experience an electrical failure. The electrical failure can be experienced during fabrication of the integrated circuit or after a period of time that the integrated circuit has

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been in use, such as where electrical contact with the conductive layer in the recess has been lost because the material of the conductive layer moves.

It would be an advantage in the art to overcome the problems of poor step coverage and voids.

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## SUMMARY OF THE INVENTION

In accordance with the invention as embodied and broadly described herein, the present invention relates to the method for manufacturing an interconnect structure situated on a semiconductor wafer having a substrate assembly thereon. A novel interconnect structure is also disclosed. The term substrate assembly is intended herein to mean a substrate having one or more layers or structures formed thereon. As such, the substrate assembly may be, by way of example and not by way of limitation, a doped silicon semiconductor substrate typical of a semiconductor wafer.

The interconnect structure is formed in a dielectric material situated on the substrate assembly of the semiconductor wafer. The novel process forms the dielectric material into a recess having a specified geometry shape. The shape formed in the dielectric material will preferably be a recess therein. The recess can be a trench, a hole, a via, or a combination of a trench and a hole or via. The dielectric shape can be formed by processing the dielectric material by way of dry etching or other recess-creating process.

Following the creation of the dielectric structure in the dielectric material, at least one diffusion barrier layer is formed over the dielectric structure. The diffusion barrier layer is at least partially conformably formed upon the dielectric structure. The material from which the diffusion barrier layer is substantially composed is preferably selected from the group consisting of ceramics, metallics, and intermetallics. More preferably, the diffusion barrier layer is substantially composed of a material that is selected from the group consisting of aluminum nitride, tungsten nitride, titanium nitride, and tantalum nitride

A seed layer is then formed upon the diffusion barrier layer. The seed layer helps to promote nucleation, deposition, and growth of a material that will be used to fill up the dielectric structure. The seed layer can also serve the purpose of increasing surface mobility of the barrier layer which helps to make a desirable filling of the dielectric structure in the metallization process. Preferably, the material from which the seed layer is substantially

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composed is selected from the group consisting of ceramics, metallics, and intermetallics. More preferably, the material from which the seed layer is composed is selected from the group consisting of aluminum, titanium nitride, titanium, and titanium aluminide. Additionally and by comparison, the diffusion barrier layer will preferably be composed of a material having a melting point greater than or equal to that of the material from which the seed layer is composed

An electrically conductive layer is then formed upon the seed layer. The electrically conductive layer is the current carrier for electrical signals that will communicate with an integrated circuit associated therewith. Preferably, the electrically conductive layer is substantially composed of aluminum or copper. The material from which the diffusion barrier layer is composed will preferably have a melting point greater than that of a material from which the electrically conductive layer is composed. The material from which the seed layer is composed will preferably have a melting point greater than or equal to that of the material from which the electrically conductive layer is composed.

An energy absorbing layer is then formed upon the conductor layer. The energy absorbing layer will preferably have a greater thermal absorption capacity than that of the electrically conductive layer. Alternatively, the energy absorbing layer will preferably being composed of a material having a higher melting point than that of the material from which the electrically conductive layer is composed. As another alternative, the energy absorbing layer will preferably be composed of a material having both a higher thermal insulation capacity and electric insulation capacity than that of the material from which the electrically conductive layer is composed.

The energy absorbing layer is heated to cause the conductor layer to flow so as to fill voids that have formed within the dielectric structure. In conjunction with the heating of the energy absorbing layer, a pressure above atmospheric pressure can be applied to the semiconductor substrate assembly to better assist the process of causing the conductor layer

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to flow so as to fill voids within the dielectric structure. Preferably, the energy absorbing layer is substantially composed of a material selected from the group consisting of titanium, titanium nitride, tungsten, tungsten nitride, silicon nitride, silicon dioxide, tantalum, tantalum nitride, and carbon.

Following the steps of heating or heating and pressurizing the energy absorbing layer, the energy absorbing layer is removed, preferably by planarizing. The planarizing step may also remove a portion of the conductive layer situated above the dielectric structure.

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## BRIEF DESCRIPTION OF THE DRAWINGS

A more particular description of the invention briefly described above will be rendered by reference to specific embodiments thereof which are illustrated in the appended drawings. Understanding that these drawings depict only typical embodiments of the invention and are not therefore to be considered to be limiting of its scope, the invention will be described and explained with additional specificity and detail through the use of the accompanying drawings in which:

Figure 1 is a partial cross-sectional elevation and perspective view of a dielectric material that is situated upon a monocrystalline silicon layer of a semiconductor wafer, the dielectric material having a dielectric structure formed therein that is shaped as a recess in the dielectric material, the recess featuring the combination of a hole extending to a trench in the dielectric material, the hole terminating at the monocrystalline silicon layer of the semiconductor wafer.

Figure 2 is a partial perspective cross-sectional elevation view of a portion of Figure 1, showing various interconnect structure, including a trench in the dielectric material, a hole in the dielectric material, and a combination thereof, each said interconnect structure having thereon one or more layers of each of a barrier layer, a seed layer, a conductive layer, and an energy absorbing layer.

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## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figure 1 depicts a semiconductor substrate assembly 10. A lower substrate known as a silicon layer 22 is formed in semiconductor substrate assembly 10, and a dielectric material 14 is upon silicon layer 22. Lower substrate or silicon layer 22 defines a plane and comprises material selected from the group consisting of silicon dioxide, silicate glass and mixtures or derivatives thereof. A hole 18 having a cylindrical shape extends from silicon layer 22 to terminate at a trench 20 formed in dielectric material 14. Trench 20 is rectangular in cross-section.

Figure 2 shows a cross-section 12 seen Figure 1. Another trench 32, and another hole 34 are also depicted. Trench 32 is not situated over a hole as is trench 20. Figure 2 also depicts a hole 34 having a triangular cross-section and extending from a top surface of dielectric material 14 to terminate at silicon layer 22. When filed with materials for a metallization process and subsequently planarized, holes 18, 34, and trenches 20, 32 become interconnect structures in the metallization process as described below.

To initiate the metallization process, dielectric material 14 is formed upon silicon layer 22 by conventional processing, such as depositing doped or undoped oxide by various CVD processes, or by TEOS deposition. Next, dielectric material 14 has recesses formed therein, including for example holes 18, 34, and trenches 20, 32, the formation of which is by conventional processing methods such as patterning and etching.

After dielectric material 14 has been processed into the desired configuration of recesses, the next step is to form a barrier layer 24 over the dielectric structure 16. Barrier layer 24 may be formed, by way of example and not by way of limitation, by multiple deposition of a material. The material from which barrier layer 24 is composed preferably will act as an adhesion layer for materials formed thereon, and also will acts as a diffusion barrier to prevent the diffusion of material through barrier layer 24.

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Barrier layer 24 will preferably be a substantially continuous coating of material over the recesses in dielectric material 14. Barrier layer 24 may be comprised of refractory metals or nitrides thereof, such as titanium, tungsten, tantalum, titanium nitride, tungsten nitride, or tantalum nitride. Typically, barrier layer 24 is titanium and/or titanium nitride together. Barrier layer 24 can be particularly important in the areas where holes 18, 34 extend past dielectric material 14 to terminate at silicon layer 22.

The next step, which may be desirable in the inventive method depending upon the composition of materials used to fill the recesses in dielectric material 14, is to thermally process barrier layer 24. The thermal processing of barrier layer 24 helps to improve electrical contact of the interconnect structures being formed. For example, if titanium is deposited, then it is desirable that a thermal process be performed. The thermal process would preferably be heating the semiconductor substrate assembly in a nitrogen environment at a selected temperature at which nitrides are formed on the surface of the titanium. If barrier layer 24 comprises titanium or titanium nitride, argon may be used as the environment for thermal processing. In this example, titanium exposed to the nitrogen environment would form titanium nitride and exposed silicon would form silicon nitride. As the thermal process heats the semiconductor substrate assembly, titanium silicide would form so as to create a desirable contact resistance with silicon layer 22.

A seed layer 26 is formed over barrier layer 24 in the next step of the inventive method. The type of material used as seed layer 26 is dependant upon subsequent processing. If some type of subsequent reflow process is needed for later added layers, or even a CVD process is going to be used for the formation of seed layer 26, seed layer 26 will preferably be formed prior to subsequent processing so as to clean barrier layer 24. The use of seed layer 26 provides a surface on barrier layer 24 that is substantially free of contaminates that may interfere with surface diffusion. Seed layer 26 promotes the deposition and growth of a layer of material that will be formed thereon. Additionally, seed

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layer 26 will preferably be the main conductor for current in the interconnect structure and will promote surface mobility of materials formed thereon so as to fill the recesses in dielectric material 14 is a desirable manner.

By way of example of materials and processes for formation of seed layer 26, a CVD tungsten process can be used. When so processed there will be a nucleation of seed layer 26 that will be rich in both silicon and hydrogen, initially. The CVD tungsten process will then preferably undergo a chemistry change in the middle thereof so as to become rich in hexflouride such that a more pure form of tungsten material makes up seed layer 26. Those of ordinary skill in the art will understand the selection of proper seed layer 26 compositions, which selection may be done empirically utilizing chemical potential differences and differences in diffusion characteristics of materials.

The seed layer may also be made of titanium nitride, which is preferred when aluminum is used in the interconnect structures. If so, the seed layer should be deposited in situ prior to filling the interconnect structures with aluminum so as to enable the aluminum to freely flow and to avoid binding up the flow of the aluminum. Multiple layers can be used to make up the seed layer, which multiple layers will preferably be deposited in a vacuum system and will be composed, for example, of both titanium nitride and/or silicon.

The next step in the inventive method is the formation of a conductor layer 28. Conductor layer 28 will preferably be composed of typical metallization conductor materials. For example, if a reflow or a fill process with aluminum process is going to be used, then an aluminum and high pressure fill would be used to substantially cover seed layer 26 in the recesses within dielectric material 14. The composition of conductor layer 28 may depend on the aspect ratio of the recesses within dielectric material 14. Aspect ratios below four (4) may not require a high pressure fill of the recesses. Another example of a conductor material is copper.

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When aluminum is used as conductor layer 28, the composition of barrier layer 24 will preferably be selected to avoid a heat induced reaction of aluminum with silicon in silicon layer 22 so as to form tetrahedrons in the silicon, wherein by a detrimental effect is realized.

An energy absorbing layer 30 is then formed, preferably by deposition, upon conductor layer 28. Energy absorbing layer 30 retains thermal energy and comprises a material that has a higher thermal conductivity than conductor layer 28. By way of example and not limitation, if conductor layer 28 is composed of aluminum and energy absorbing layer 30 is composed of tungsten, the tungsten has a higher melting point that aluminum. This results in the tungsten retaining more energy.

From a spectral point of view, if aluminum is used as conductor layer 28 and depending how the aluminum layer is deposited, it is possible to obtain something that is not as spectrally reflective. A preferable characteristic of energy absorbing layer 30 is that it must be able to absorb more energy than the material that is used as conductor layer 28. The purpose behind this requirement is that when challenging structures (e.g. recesses in dielectric material 14 having aspect ratios greater than four (4) to one (1) are being formed which are to be filled with a conductor, the conductor will flow more freely to fill a recess when thermal energy is retained within the conductor by a layer thereon that will better retain such thermal energy. As such, the flowablility of the conductor is enhanced so that diffusion thereof into the recess is bettered.

Enhancing the diffusion characteristics of the material of the conductor is achieved by either volume diffusion or surface diffusion, each of which are time and temperature dependent. The temperature of the conductor is held high for at a longer period of time while underlying or overlying materials retain thermal energy. The formation of energy absorbing layer 30 on conductor layer 28 substantially retains thermal energy under an interfacial

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surface of energy absorbing layer 30 so that the thermal energy can diffuse into conductor layer 28.

By way of example, if conductor layer 28 is aluminum, energy absorbing layer 30 can be titanium nitride, tungsten, or even a dielectric substance. A layer of titanium nitride is less thermally conductive than aluminum. If conductor layer 28 is copper, examples of energy absorbing layers 30 are tungsten, titanium nitride, tantalum or carbon.

The next step of the inventive method is to apply energy to energy absorbing layer 30. The energy that is applied to energy absorbing layer 30 is transmitted to conductor layer 28. Conductor layer 28 is then able to flow and fill voids that have formed in recesses within dielectric material 14. With the voids removed, desirable step coverage of the recesses within dielectric material 14, and desirable fill of the recesses is achieved. Examples of ways to apply energy to energy absorbing layer 30 include, but are not limited to, lasers, tube furnaces, RTP or other kinds of radiant or thermal energy. Preferably, energy absorbing layer 30 will be heated.

A preferable step that follows the forgoing steps is the removal of materials from the semiconductor substrate assembly by an abrasive planarizing process, for example, chemical mechanical planarizing. Material will be removed during the planarizing process until planarization line 36 seen in Figure 2 is reached. The resulting interconnect structures have been metallized so as to be buried within dielectric material 14, and as such can be considered to be a metallization by "wire-down" technology. Subsequent and conventional processing can then following in the fabrication processing of the semiconductor substrate assembly.

Figure 2 shows a novel dual damescene structure depicted as hole 18 and trench 20 filled with each of barrier layer 24, seed layer 26, and conductor layer 28, where trench 20 has been planarized at planarization line 36. Planarization line 36 makes the metallization

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in an "inlaid" form. The two or "dual" metallization damescene structure is seen in the inlaid combination of both hole 18 and trench 20.

The disclosed novel method is capable of desirable step coverage and being capable of filling in a recess within a dielectric material having an aspect ratio greater than about four (4) to one (1). As such, the novel process improves both the yield and reliability over conventional processes.

The present invention may be embodied in other specific forms without departing from its spirit or essential characteristics. The described embodiments are to be considered in all respects only as illustrated and not restrictive. The scope of the invention is, therefore, indicated by the appended claims rather than by the foregoing description. All changes which come within the meaning and range of equivalency of the claims are to be embraced within their scope.

What is claimed and desired to be secured by United States Letters Patent is:

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1. A method for manufacturing an interconnect structure comprising the steps of:

forming a recess within a dielectric material situated on a semiconductor lower substrate, said recess extending below a top surface of said dielectric material;

forming a diffusion barrier layer on the recess within the dielectric material;

forming a seed layer on the diffusion barrier layer, the diffusion barrier layer being composed of a material having a melting point greater than or equal to that of a material from which the seed layer is composed;

forming an electrically conductive layer on the seed layer, the material from which the diffusion barrier layer is composed having a melting point greater than that of a material from which the electrically conductive layer is composed, the material from which the seed layer is composed having a melting point greater than or equal to that of the material from which the electrically conductive layer is composed;

forming an energy absorbing layer on said electrically conductive layer, said energy absorbing layer having a greater thermal absorption capacity than that of said electrically conductive layer;

applying energy to said energy absorbing layer so to as heat said electrically conductive layer and to cause said electrically conductive layer to flow within said recess; and

removing portions of the energy absorbing layer and the electrically conductive layer that are situated above the top surface of the dielectric material.

2. A method for manufacturing an interconnect structure as recited in Claim 1, wherein the step of forming a diffusion barrier layer on the recess within the dielectric material is a CVD deposition step.

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3. A method for manufacturing an interconnect structure as recited in Claim 1, wherein the material from which the diffusion barrier layer is substantially composed is selected from the group consisting of ceramics, metallics, and intermetallics.

4. A method for manufacturing an interconnect structure as recited in Claim 1, wherein the material from which the diffusion barrier layer is composed is selected from the group consisting of aluminum nitride, tungsten nitride, titanium nitride, and tantalum nitride.

5. A method for manufacturing an interconnect structure as recited in Claim 1, further comprising the step, prior to the step of forming a seed layer on the diffusion barrier layer, of heating the diffusion barrier layer is an environment substantially containing a nitrogen gas.

6. A method for manufacturing an interconnect structure as recited in Claim 1, wherein the step of depositing a seed layer on the diffusion barrier layer is a CVD deposition step.

7. A method for manufacturing an interconnect structure as recited in Claim 1, wherein the material from which the seed layer is substantially composed is selected from the group consisting of ceramics, metallics, and intermetallics.

8. A method for manufacturing an interconnect structure as recited in Claim 1, wherein the material from which the seed layer is composed is selected from the group consisting of aluminum, titanium nitride, titanium, and titanium aluminide.

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9. A method for manufacturing an interconnect structure as recited in Claim 1, wherein the material from which the electrically conductive layer is composed is selected from the group consisting of aluminum and copper.

10. A method for manufacturing an interconnect structure as recited in Claim 1, wherein the energy absorbing layer is substantially composed of a material selected from the group consisting of titanium, titanium nitride, tungsten, tungsten nitride, silicon nitride, silicon dioxide, tantalum, tantalum nitride, and carbon.

11. A method for manufacturing an interconnect structure as recited in Claim 1, wherein the step of applying energy to said energy absorbing layer to heat the energy absorbing layer utilizes at least one energy source selected from the group consisting of a laser, a furnace, and an RTP lamp.

12. A method for manufacturing an interconnect structure as recited in Claim 1, wherein said step of removing portions of the energy absorbing layer and the electrically conductive layer is an abrasive planarization step.

13. A method for manufacturing an interconnect structure as recited in Claim 12, wherein said step of removing portions of the energy absorbing layer and the electrically conductive layer is a chemical mechanical planarizing step.

14. A method for manufacturing an interconnect structure as recited in Claim 1, wherein the recess has an aspect ratio greater than about four (4) to one (1).

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15. A method for manufacturing an interconnect structure as recited in Claim 1, wherein the recess comprises a contact hole situated below a trench, said semiconductor substrate assembly having a lower substrate defining a plane, said contact hole terminating at an end thereof at said lower substrate and terminating at an opposite end thereof at said trench, said trench extending from said opposite end of said contact hole to a top surface of said dielectric material, the trench extending substantially parallel to the plane of the lower substrate.

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16. A method for manufacturing an interconnect structure comprising the steps of:

patterning and etching a dielectric material situated on a semiconductor substrate assembly so as to form a recess within the dielectric material, said recess being situated below a top surface of said dielectric material;

depositing a diffusion barrier layer within the recess within the dielectric material, the diffusion barrier layer being composed of a material selected from the group consisting of ceramics, metallics, and intermetallics;

depositing a seed layer on the diffusion barrier layer, the seed layer being composed of a material selected from the group consisting of ceramics, metallics, and intermetallics, the material from which the diffusion barrier layer is composed having a melting point greater than or equal to that of the material from which the seed layer is composed;

depositing an electrically conductive layer on the seed layer, the material from which the diffusion barrier layer is composed having a melting point greater than that of the material from which the electrically conductive layer is composed, the material from which the seed layer is composed having a melting point greater than or equal to that of the material from which the electrically conductive layer is composed;

depositing an energy absorbing layer on said electrically conductive layer, said energy absorbing layer being composed of a material having a higher melting point than that of the material from which the electrically conductive layer is composed;

heating the energy absorbing layer so to as heat the conductive layer and to cause said conductive layer to flow within said recess; and

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planarizing the semiconductor substrate assembly so as to remove those portions of the energy absorbing layer and the electrically conductive layer that are situated above the top surface of the dielectric material.

17. A method for manufacturing an interconnect structure as recited in Claim 16, wherein the material from which the diffusion barrier layer is composed is selected from the group consisting of aluminum nitride, tungsten nitride, titanium nitride, and tantalum nitride.

18. A method for manufacturing an interconnect structure as recited in Claim 16, wherein the material from which the seed layer is composed is selected from the group consisting of aluminum, titanium nitride, titanium, and titanium aluminide.

19. A method for manufacturing an interconnect structure as recited in Claim 16, wherein the material from which the electrically conductive layer is composed is selected from the group consisting of aluminum and copper.

20. A method for manufacturing an interconnect structure as recited in Claim 16, wherein the energy absorbing layer is substantially composed of a material selected from the group consisting of titanium, titanium nitride, tungsten, tungsten nitride, silicon nitride, silicon dioxide, tantalum, tantalum nitride, and carbon.

21. A method for manufacturing an interconnect structure as recited in Claim 16, wherein the recess has an aspect ratio greater than about 4 to 1.

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22. A method for manufacturing an interconnect structure as recited in Claim 16, wherein the recess comprises a contact hole situated below a trench, said semiconductor substrate assembly having a lower substrate defining a plane, said contact hole terminating at an end thereof at said lower substrate and terminating at an opposite end thereof at said trench, said trench extending from said opposite end of said contact hole to a top surface of said dielectric material, the trench extending substantially parallel to the plane of the lower substrate.

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23. A method for manufacturing an interconnect structure comprising the steps of:

patterning and etching a dielectric material situated on a semiconductor substrate assembly so as to form a recess within the dielectric material, said recess being situated below a top surface of said dielectric material;

depositing a diffusion barrier layer within the recess within the dielectric material, the diffusion barrier layer being composed of a material selected from the group consisting of aluminum nitride, tungsten nitride, titanium nitride, and tantalum nitride;

depositing a seed layer on the diffusion barrier layer, the seed layer being composed of a material selected from the group consisting of aluminum, titanium nitride, titanium, and titanium aluminide, the material from which the diffusion barrier layer is composed having a melting point greater than or equal to that of the material from which the seed layer is composed;

depositing an electrically conductive layer on the seed layer, the material from which the diffusion barrier layer is composed having a melting point greater than that of a material from which the electrically conductive layer is composed, the material from which the seed layer is composed having a melting point greater than or equal to that of the material from which the electrically conductive layer is composed, the material from which the electrically conductive layer is composed is selected from the group consisting of aluminum and copper;

depositing an energy absorbing layer on said electrically conductive layer, said energy absorbing layer being composed of a material having a higher melting point than that of the material from which the electrically conductive layer is composed, the energy absorbing layer being is substantially composed of a material

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selected from the group consisting of titanium, titanium nitride, tungsten, tungsten nitride, silicon nitride, silicon dioxide, tantalum, tantalum nitride, and carbon;

heating the energy absorbing layer so to as heat the conductive layer and to cause said conductive layer to flow within said recess; and

planarizing the semiconductor substrate assembly so as to remove those portions of the energy absorbing layer and the electrically conductive layer that are situated above the top surface of the dielectric material.

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24. A method for manufacturing an interconnect structure comprising the steps of:

forming a dielectric material on a monocrystalline silicon layer of a semiconductor substrate assembly, said monocrystalline silicon layer defining a plane;

patterning and etching the dielectric material so as to form a recess within said dielectric material, said recess comprising a contact hole situated below a trench, said contact hole terminating at an end thereof at the silicon layer and terminating at an opposite end thereof at said trench, said trench extending from said opposite end of said contact hole to a top surface of said dielectric material, the trench being substantially parallel to the plane of the monocrystalline silicon layer;

depositing a diffusion barrier layer within the recess within the dielectric material, the diffusion barrier layer being composed of a material selected from the group consisting of ceramics, metallics, and intermetallics;

depositing a seed layer on the diffusion barrier layer, the seed layer being composed of a material selected from the group consisting of ceramics, metallics, and intermetallics, the material from which the diffusion barrier layer is composed having a melting point greater than or equal to that of the material from which the seed layer is composed;

depositing a layer substantially composed of aluminum on the seed layer, the material from which the diffusion barrier layer is composed having a melting point greater than that of aluminum, the material from which the seed layer is composed having a melting point greater than or equal to that of aluminum;

depositing an energy absorbing layer on said electrically conductive layer, said energy absorbing layer being composed of a material having both a higher

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thermal insulation capacity and electric insulation capacity than that of the material from which the electrically conductive layer is composed;

heating the energy absorbing layer so to as heat the conductive layer and to cause said conductive layer to flow within said recess; and

planarizing the semiconductor substrate assembly so as to remove those portions of the energy absorbing layer and the electrically conductive layer that are situated above the top surface of the dielectric material.

25. A method for manufacturing an interconnect structure as recited in Claim 24, wherein the material from which the diffusion barrier layer is composed is selected from the group consisting of aluminum nitride, tungsten nitride, titanium nitride, and tantalum nitride.

26. A method for manufacturing an interconnect structure as recited in Claim 24, wherein the material from which the seed layer is composed is selected from the group consisting of aluminum, titanium nitride, titanium, and titanium aluminide.

27. A method for manufacturing an interconnect structure as recited in Claim 24, wherein the material from which the energy absorbing layer is substantially composed is selected from the group consisting of titanium, titanium nitride, tungsten, tungsten nitride, silicon nitride, silicon dioxide, tantalum, tantalum nitride, and carbon.

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28. A method for manufacturing an interconnect structure comprising the steps of:

forming at least one silicon layer on a monocrystalline silicon layer of a semiconductor substrate assembly, said silicon layer being selected from the group consisting of undoped silicon dioxide, doped silicon dioxide, undoped silicate glass, and doped silicate glass, wherein said monocrystalline silicon layer defines a plane;

patterning and etching the at least one silicon dioxide layer so as to form a recess therein, said recess comprising a contact hole situated below a trench, said contact hole terminating at an end thereof at the at least one silicon layer and terminating at an opposite end thereof at said trench, said trench extending from said opposite end of said contact hole to a top surface of said at least one silicon layer, the trench being substantially parallel to the plane of the monocrystalline silicon layer;

depositing a diffusion barrier layer within the recess within the at least one silicon layer, the diffusion barrier layer being composed of a material selected from the group consisting of aluminum nitride, tungsten nitride, titanium nitride, and tantalum nitride;

depositing a seed layer on the diffusion barrier layer, the seed layer being composed of a material selected from the group consisting of aluminum, titanium nitride, titanium, and titanium aluminide, the material from which the diffusion barrier layer is composed having a melting point greater than or equal to that of the material from which the seed layer is composed;

depositing a layer substantially composed of aluminum on the seed layer, the material from which the diffusion barrier layer is composed having a melting point greater than that of aluminum, the material from which the seed layer is composed having a melting point greater than or equal to that of aluminum;

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depositing an energy absorbing layer on said electrically conductive layer, said energy absorbing layer being composed of a material having both a higher thermal insulation capacity and electric insulation capacity than that of the material from which the electrically conductive layer is composed, the material from which the energy absorbing layer is substantially composed is selected from the group consisting of titanium, titanium nitride, tungsten, tungsten nitride, silicon nitride, silicon dioxide, tantalum, tantalum nitride, and carbon;

heating the energy absorbing layer so to as heat the conductive layer and to cause said conductive layer to flow within said recess; and

planarizing the semiconductor substrate assembly so as to remove those portions of the energy absorbing layer and the electrically conductive layer that are situated above the top surface of the at least one silicon layer.

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29. An interconnect structure comprising:

a lower substrate situated on a semiconductor substrate assembly, said lower substrate defining a plane;

a dielectric material on the lower substrate having a planar top surface;

a recess within said dielectric material, said recess comprising a contact hole situated below a trench, said contact hole terminating at an end thereof at the lower substrate and terminating at an opposite end thereof at said trench, said contact hole being oriented substantially perpendicular to the plane of said lower substrate, said trench extending from said opposite end of said contact hole to a top surface of said dielectric material, the trench extending substantially parallel to the plane of said lower substrate; and

an electrically conductive layer situated within and filling both the contact hole and the trench and extending to terminate at the planar top surface of the dielectric material.

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30. An interconnect structure comprising:

a lower substrate situated on a semiconductor substrate assembly, said lower substrate defining a plane;

a dielectric material on the lower substrate having a planar top surface;

a recess within said dielectric material, said recess comprising a contact hole situated below a trench, said contact hole terminating at an end thereof at the silicon layer and terminating at an opposite end thereof at said trench, said contact hole being oriented substantially perpendicular to the plane of said lower substrate, said trench extending from said opposite end of said contact hole to a top surface of said dielectric material, the trench extending substantially parallel to the plane said lower substrate;

a diffusion barrier layer on the trench and the contact hole;

a seed layer on the diffusion barrier layer, the diffusion barrier layer being composed of a material having a melting point greater than or equal to that of a material from which the seed layer is composed; and

an electrically conductive layer on the seed layer and extending to terminate at the planar top surface of the dielectric material, the material from which the diffusion barrier layer is composed having a melting point greater than that of a material from which the electrically conductive layer is composed, the material from which the seed layer is composed having a melting point greater than or equal to that of the material from which the electrically conductive layer is composed.

31. An interconnect structure as defined in Claim 30, wherein the material from which the diffusion barrier layer is substantially composed is selected from the group consisting of aluminum nitride, tungsten nitride, titanium nitride, and tantalum nitride.

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32. An interconnect structure as defined in Claim 30, wherein the material from which the seed layer is substantially composed is selected from the group consisting of aluminum, titanium nitride, titanium, and titanium aluminide.

33. An interconnect structure as defined in Claim 30, wherein the material from which the electrically conductive layer is substantially composed is selected from the group consisting of aluminum and copper.

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34. An interconnect structure comprising:

a monocrystalline silicon layer of a semiconductor substrate assembly, said monocrystalline silicon layer defining a plane;

a dielectric material on the monocrystalline silicon layer;

a recess within said dielectric material, said recess comprising a contact hole situated below a trench, said contact hole terminating at an end thereof at the silicon layer and terminating at an opposite end thereof at said trench, said contact hole being oriented substantially perpendicular to the plane of said monocrystalline silicon layer, said trench extending from said opposite end of said contact hole to a top surface of said dielectric material, the trench extending substantially parallel to the plane of said monocrystalline silicon layer;

a diffusion barrier layer on the trench and the contact hole, the diffusion barrier layer being substantially composed of a material selected from the group consisting of aluminum nitride, tungsten nitride, titanium nitride, and tantalum nitride;

a seed layer on the diffusion barrier layer, the seed layer being substantially composed of a material selected from the group consisting of aluminum, titanium nitride, titanium, and titanium aluminide, the material from which the diffusion barrier layer is composed having a melting point greater than or equal to that of the material from which the seed layer is composed; and

an electrically conductive layer on the seed layer and extending to terminate at the planar surface of the dielectric material, the material from which the diffusion barrier layer is composed having a melting point greater than that of the material from which the electrically conductive layer is composed, the material from which the seed layer is composed having a melting point greater than or equal to that of the material from which the electrically conductive layer is composed, the material from

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which the electrically conductive layer is substantially composed being selected from the group consisting of aluminum and copper.

35. An interconnect structure recited in Claim 34, wherein the contact hole has an aspect ratio greater than about 4 to 1.

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## ABSTRACT OF THE INVENTION

Disclosed is a method for manufacturing an interconnect structure situated on a semiconductor wafer having a substrate assembly thereon. The interconnect structure is formed in a recess such as a trench, a hole, a via, or a combination of a trench and a hole or via within a dielectric material situated on the substrate assembly of the semiconductor wafer. At least one barrier layer is deposited within the recess. A seed layer helping to promote nucleation, deposition, and growth of a material that will be used to fill up the recess is then deposited on the barrier layer. An electrically conductive layer is then formed upon the seed layer. An energy absorbing layer will then be formed upon the conductor layer, where the energy absorbing layer has a greater thermal absorption capacity than that of the electrically conductive layer. The energy absorbing layer is heated, with or without an applied heightened pressure, to cause the conductor layer to flow so as to fill voids that have formed within the dielectric structure. Following the steps of heating or heating and pressurizing the energy absorbing layer, both the energy absorbing layer and a portion of the conductive layer situated above the dielectric structure are removed.

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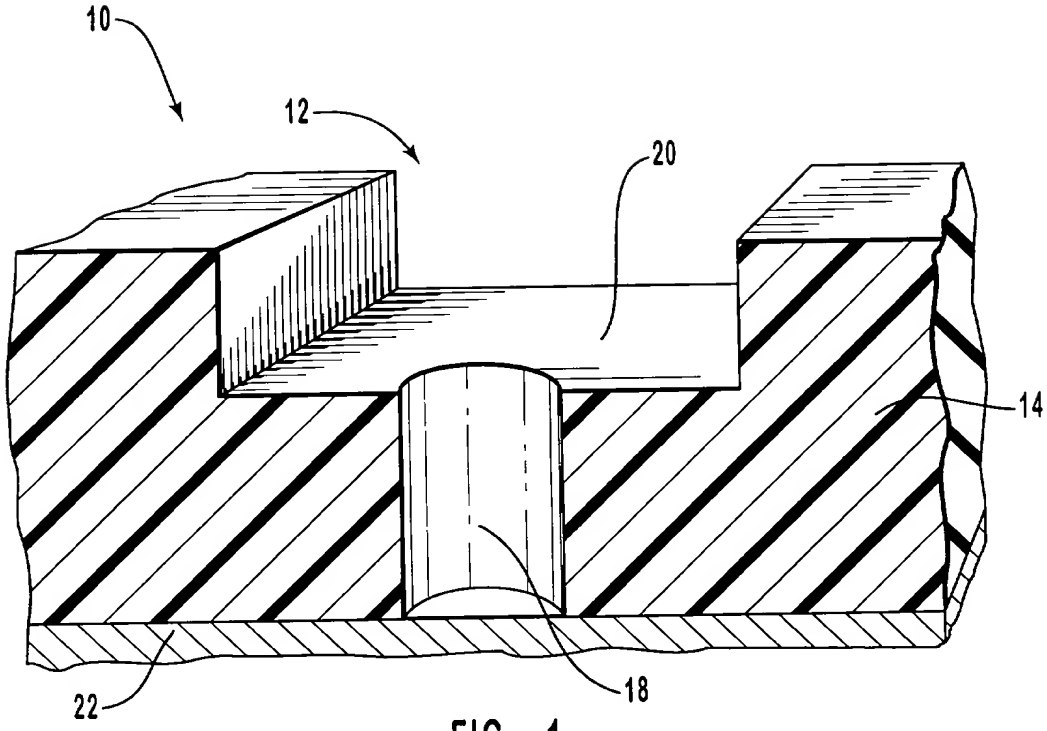


FIG. 1

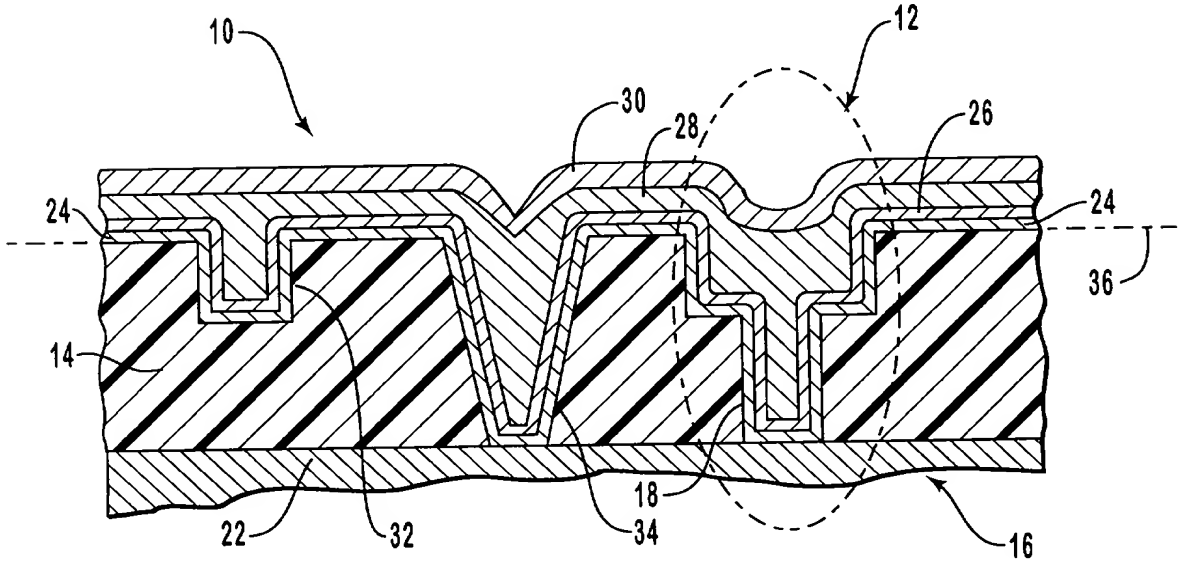


FIG. 2

Express Mailing Label No. EM246228404US

PATENT APPLICATION
Docket No: 11675.106

DECLARATION, POWER OF ATTORNEY, AND PETITION

I, John H. Givens, declare: that I am a citizen of the United States of America; that my residence and post office address is 3030 West Bonner Street, Meridian, Idaho 83712; that I verily believe I am the original, first, and sole inventor of the subject matter of the invention or discovery entitled UTILIZATION OF ENERGY ABSORBING LAYER TO IMPROVE METAL FLOW AND FILL IN A NOVEL INTERCONNECT STRUCTURE for which a patent is sought and which is described and claimed in the specification attached hereto; that I have reviewed and understand the contents of the above-identified specification, including the claims referred to, and that I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Section 1.56(a) of Title 37 of the Code of Federal Regulations.

I declare further that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful, false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful, false statements may jeopardize the validity of the application or any patent issuing thereon.

I hereby appoint as my attorneys and/or patent agents: H. ROSS WORKMAN, Registration No. 25,230; RICK D. NYDEGGER, Registration No. 28,651; DAVID O. SEELEY, Registration No. 30,148; KENT S. BURNINGHAM, Registration No. 30,453; TODD E. ZENGER, Registration

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Bradley K. DeSandro, Attorney
WORKMAN, NYDEGGER & SEELEY
1000 Eagle Gate Tower
60 East South Temple
Salt Lake City, Utah 84111

Wherefore, I pray that Letters Patent be granted to me for the invention or discovery described and claimed in the foregoing specification and claims, declaration, power of attorney, and this petition.

Signed at Boise, Idaho, this 6 day of February, 1997.

Inventor: John H. Givens

John H. Givens
3030 West Bonner Street
Meridian, Idaho 83712

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